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(71) Applicant: NATIONAL SEMICONDUCTOR CORPORATION [US/US]; 2900 Semiconductor Drive, M/S 16-135, Santa Clara, CA 95052 (US).

(72) Inventor: BERGEMONT, Albert; 5512 Castle Glen Avenue, Santa Clara, CA 95014 (US).

(74) Agent: RODDY, Richard, J.; National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, CA 95052-8090 (US).

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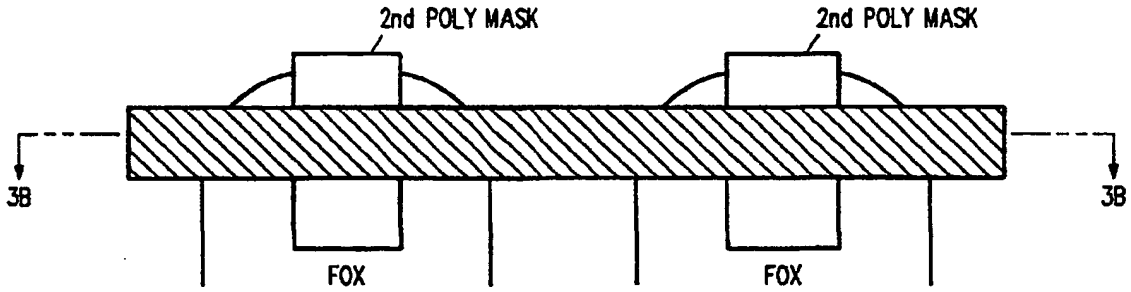

(57) Abstract

A two step mask/etch process for fabricating a poly end cap on field oxide begins with the formation of a layer of polysilicon (106) over the field oxide island (100) and over the gate oxide material (104) on the substrate (102) such that the layer of polysilicon (106) spans the interface between the substrate (102) and the field oxide (100). In a first mask/etch step, the layer of polysilicon is patterned utilizing a photoresist mask to form a line of polysilicon that extends in the x-direction such that the two longitudinal edges of the line are formed over the field oxide and such that the line extends over the field oxide in the x-direction. In a second mask/etch step, the line of polysilicon (106) is patterned utilizing a photoresist mask (108) to define a substantially rectangular poly end cap over the field oxide (100).

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METHOD OF ELIMINATING POLY END CAP ROUNDING EFFECT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to integrated circuit fabrication techniques and, in particular, to a method of fabricating polysilicon lines that terminate on field oxide in way that eliminates the potential leakage path resulting from the rounding effect of the poly end cap.

2. Discussion of the Prior Art

In many integrated circuit structures, such as CMOS logic for example, it is common to utilize polysilicon lines that terminate on field oxide.

According to conventional single poly integrated circuit fabrication techniques, all of the polysilicon lines in the circuit are defined simultaneously utilizing a single mask step. That is, a layer of polysilicon (poly1) is first formed over the entire device structure. A poly1 photoresist mask is then formed and patterned to define the underlying polysilicon. A single etch step is then performed to define individual poly1 lines.

As shown in Fig. 1A, the fabrication process specification defines the desired offset distances "a" and "b" for the "end caps" of the individual polysilicon lines in both the x-direction and the y-direction, respectively.

However, rather than the substantially rectangular (90°) geometry shown in Fig. 1A, in reality, the final geometry of both the field oxide island 10 and the end cap of the polysilicon line 12 is more "rounded", as shown in Fig. 1B. The field oxide rounding effect is inherent to the type of field isolation and photolithographic process used. The poly end cap rounding effect is inherent to the photolithography of small polysilicon lines.

As shown in Fig. 1B, these physical rounding effects result in a reduced width of the polysilicon lines 10 at the poly1/field oxide interface. Thus, when the poly1 line is used as a self-aligned mask for the implementation of dopant to create the source and drain regions of MOS transistors in the circuit, the channel length of the MOS device is reduced, leading to undesirable current leakage from one side of the poly1 to the other. Any misalignment of the poly1 mask further exacerbates this leakage problem, as shown in Fig. 1C.

To avoid this problem, prior art techniques rely on larger design rules. That is, design rules for the length of the poly end cap, the distance between the poly end cap and the parallel edge of the field oxide, and the width of the poly1 line all may be increased. These steps insure that the channel length of each of the MOS devices in the circuit is greater than an acceptable minimum required to prevent leakage.

However, this approach is totally antithetical to the concept of design scaling, with the final result being a larger integrated circuit die.

Therefore, it would be highly desirable to have available a method of fabricating polysilicon lines for termination on field oxide in a manner that is consistent with the objective of design rule scaling and smaller die size.

SUMMARY OF THE INVENTION

The present invention provides a method of fabricating a polysilicon line over an interface between field oxide and adjacent silicon substrate material. The silicon substrate material typically has gate xide formed thereon. In accordance with the method, a layer of polysilicon is formed over the field oxide and over the gate oxide material such that the layer of polysilicon spans the interface between the field oxide

and the substrate underlying the gate xide. In a first mask/etch step, the polysilicon layer is patterned to form a line of polysilicon such that the two longitudinal edges of the line are formed over the field oxide and such that the line extends over the field oxide. In a second mask/etch step, the polysilicon line is patterned to terminate over the field oxide to provide a substantially rectangular end cap.

These and other features and advantages of the present invention will become apparent and appreciated by reference to the detailed description of a preferred embodiment provided below which should be considered in conjunction with the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

Fig. 1A is a layout drawing illustrating the end cap of a polysilicon line formed on a field oxide island.

Fig. 1B is a layout drawing illustrating the rounding effect of field oxide isolation material and a poly end cap.

Fig. 1C is a layout drawing illustrating the problem of current leakage between a field oxide island and a poly end cap resulting from the rounding effect of each and from misalignment of the poly1 mask.

Fig. 2A is a layout drawing illustrating a first mask/etch step in patterning a polysilicon line to terminate over field oxide in accordance with the present invention.

Fig. 2B is a cross-section drawing illustrating the Fig. 2A structure along line 2B-2B in Fig. 2A.

Fig. 3A is a layout drawing illustrating a second mask/etch step in patterning a polysilicon line to terminate over field oxide in accordance with the present invention.

Fig. 3B is a cross-section drawing illustrating the Fig. 3A structure along line 3B-3B in Fig. 3A.

Fig. 4A is a layout drawing illustrating a final structure resulting from patterning a polysilicon line over field oxide in accordance with the present invention.

Fig. 4B is a cross-section drawing illustrating the Fig. 4A structure along line 4B-4B in Fig. 4A.

Fig. 5A and 5B are layout drawings illustrating the application of a two-step mask/etch process in accordance with the present invention to polysilicon lines of irregular geometry.

Fig. 6A is a layout drawing illustrating a portion of a flash EPROM memory array that utilizes polysilicon floating gate strips extending between two field oxide isolation regions to define an individual memory cell.

Fig. 6B is a cross-section drawing illustrating an individual memory cell of the Fig. 6A array that includes a polysilicon floating gate extending between two regions of field oxide.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a two-step mask/etch process for fabricating polysilicon lines over an interface between a silicon dioxide field oxide isolation region and adjacent silicon substrate material.

Referring to Figs. 2A and 2B, a process in accordance with the present invention begins with the definition of field oxide isolation regions 100 in a substrate 102 of semiconductor material, illustrated in Fig. 2B as being silicon of P-type conductivity. The field oxide regions 100 are formed in accordance with procedures well known in the art of integrated circuit fabrication. Formation of the field oxide regions 100 is followed by the formation of gate oxide material 104 in the so-called active device regions between field oxide regions 100. A layer of polysilicon is then formed over the entire above-described structure, including the field oxide regions 100 and the silicon dioxide gate material 104, such that the layer of polysilicon spans the interface between P-type substrate material 102 underlying the gate oxide 104 and the field oxide regions 100.

Next, as shown in Fig. 2A and in accordance with the present invention, in a first mask/etch step, the layer of polysilicon is masked with photoresist and patterned in accordance with conventional photolithographic techniques to a form a line 106 of polysilicon that extends in the x-direction such that

the two longitudinal edges of the line 106 are formed over the field oxide regions 100 and such that the line 106 extends over the field oxide region 100 in the x-direction.

Next, as shown in Figs. 3A and 3B, a second photoresist mask is formed over the above-described structure and patterned to expose portions of the polysilicon line 106 overlying field oxide regions 100.

Referring to Figs. 4A and 4B, finally, in a second mask/etch step and in accordance with the present invention, the polysilicon line 106 is patterned to terminate over the field oxide regions 100 to define polysilicon end caps 110 over the field oxide 100.

Utilization of this two-step mask/etch process results in the formation of substantially rectangular (90°) corners on the poly1 end caps, thus avoiding the leakage problems that result from the rounding effect described in the background section of this document.

Those skilled in the art will appreciate that the above-described process can be utilized to pattern polysilicon lines having geometries other than the "straight-line" geometry shown in Figs. 2A and 2B. For example, as shown in Figs. 5A and 5B, the original poly1 layer may be patterned in the first mask/etch step to provide polysilicon lines of irregular shape; the second mask/etch step then defines the substantially rectangular poly end caps over the field oxide.

The above-described two-step mask/etch process may also be applied advantageously in other integrated circuit structures.

Fig. 6A shows a layout of a portion 200 of a well-known, contactless flash EPROM cell array. In the illustrated array 200, individual EPROM cells are defined by the transverse crossing of a polysilicon (poly1) floating gate 202 and an overlying polysilicon (poly2) word line 204.

As shown in the Fig. 6A cross-section of an individual cell in the array 200, the word line 204 is electrically separated from the floating gate 202 by an intermediate layer of dielectric material 206, typically an oxide/nitride/oxide (ONO) sandwich. The floating gate 202 is electrically separated from the P-type silicon substrate 208 by a layer of gate oxide material 210.

Referring back to Fig. 6A, in each cell in the array 200, the floating gate 202 is flanked on each side by a buried n+ bit line 212 formed in the silicon substrate 208. The n+ bit lines 212, which provide the source and drain regions of the individual cells of the array, are separated by p-channel substrate material that underlies the floating gate 202. The individual cells in the array 200 are electrically isolated from one another by field oxide (FOX) islands 214.

As best shown in Fig. 6B, the polysilicon floating gate 202 is typically fabricated to terminate over the field oxide islands 214 in order to prevent current leakage between adjacent n+ bit lines 212 when the array 200 is subjected to certain operating bias conditions. The floating gate 202 is defined in a stacked etch step utilizing the poly2 word line 212 as a self-aligned mask.

Although the above-described stack etched process utilizes only two photoresist masks to define both the poly2 word line and the underlying poly1 floating gates of the individual memory cells, word line dimensions must be conservative in order to ensure proper definition of the floating gates. Thus, the word line design rules inhibit aggressive design scaling.

While requiring a more complex three-mask process, the concepts of the present invention can be utilized to permit further scaling in such memory architectures.

More specifically, in a method of fabricating a non-volatile memory cell array in accordance with the present invention, an x-y matrix of silicon dioxide field oxide isolation regions is formed in a surface of a P-type silicon substrate to define active device substrate regions. The active device substrate regions will subsequently be utilized for the formation of individual floating gate memory cells. A layer of silicon dioxide gate material is formed on the exposed surfaces of the active device region. A first layer of polysilicon is then formed over the field oxidized isolation regions and over the silicon dioxide gate material and a layer of oxide/nitride/oxide (ONO) is formed over the first polysilicon layer. Next, in a first mask/etch step, the ONO layer and the poly1 layer are patterned utilizing a first photoresist mask to

form a plurality of lines of ONO/poly1 that extend in the wide direction such that, for each ONO poly1 line, the two longitudinal edges of the line are formed over the silicon dioxide field oxide isolation regions, thereby defining a column of isolation regions in the x-y matrix. Arsenic implant is then performed to introduce n-type dopant to the active device regions adjacent the ONO/poly1 lines. Next, in a second mask/etch step, the ONO/poly1 lines are patterned utilizing a second photoresist mask to form a gap in the lines over each of the field oxide regions in each of the columns isolation regions to define the polysilicon floating gates of the memory cells in a corresponding array column. A second layer of polysilicon is then formed over the structure resulting from the aforementioned steps. Next, a third mask/etch step, a second layer of polysilicon is patterned using a third photoresist mask to define a plurality of word lines running in the x-direction, one such word line running perpendicular to and overlying the polysilicon floating gates in each array row. Processing of the memory array structure then proceeds to completion in accordance with conventional integrated circuit fabrication techniques.

It should be understood that various alternatives to the embodiment of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention and that methods within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. A method of fabricating a line of conductive material over an interface between a field isolation region and adjacent semiconductor substrate material, the adjacent substrate material having dielectric material formed thereon, the line of conductive material running in an x-direction, the method comprising the steps of:

forming a layer of conductive material over the field isolation region and over the dielectric material such that the layer of conductive material spans the interface between the field isolation region and the substrate material underlying the dielectric material;

in a first mask/etch step, patterning the layer of conductive material utilizing a photolithographic mask to form a line of conductive material that extends in the x-direction such that the two longitudinal edges of the line are formed over the field isolation region; and

in the second mask/etch step, patterning the line of conductive material utilizing a photolithographic mask to define a substantially rectangular end cap of conductive material over the dielectric material.

2. A method of fabricating a line of polysilicon over an interface between a silicon dioxide field oxide isolation region and adjacent silicon substrate material, the adjacent silicon substrate material having silicon dioxide gate material formed thereon, the line of polysilicon running in an x-direction, the method comprising the steps of:

forming a layer of polysilicon over the silicon dioxide field oxide region and over the silicon dioxide gate material such that the layer of polysilicon spans the interface between the silicon dioxide field oxide region and the silicon substrate material underlying the silicon dioxide gate material;

in a first mask/etch step, patterning the layer of polysilicon utilizing a photoresist mask to form a line of polysilicon that extends in the x-direction such that the two longitudinal edges of the line are formed over the silicon dioxide field oxide region; and

in a second mask/etch step, patterning the line of polysilicon utilizing a photoresist mask to define a substantially rectangular poly end cap over the silicon dioxide field oxide region.

3. A method of fabricating a non-volatile memory cell array in a silicon substrate, the memory cell array defined by a matrix of a plurality of rows of floating gate memory cells extending in an x-direction and a plurality of columns of floating gate memory cells extending in a y-direction, the fabrication method comprising the steps of:

forming an x-y matrix of silicon dioxide field oxide isolation regions in a surface of the silicon substrate to define active device substrate regions in the silicon substrate wherein the floating gate memory cells are to be subsequently formed;

forming a layer of silicon dioxide gate material on the exposed surface of the active device regions;

forming a first layer of polysilicon over the field oxide isolation regions and over the silicon dioxide gate material;

forming a layer of oxide/nitride/oxide (ONO) on the first layer of polysilicon:

in a first mask/etch step, patterning the ONO layer and the first layer of polysilicon utilizing a first photoresist mask to form a plurality of lines of ONO/poly1 that extend in the y-direction such that, for each ONO/poly1 line, the two longitudinal edges f said line are formed over the silicon dioxide field oxide isolation regions defining a column of said isolation regions in said x-y matrix of isolation regions;

introducing dopant of a conductivity type opposite the conductivity type of the silicon substrate into the active device regions adjacent the ONO/poly1 lines;

in a second mask/etch step, patterning each ONO/poly1 line utilizing a second photoresist mask to form a gap in said line over each of the field oxide region in said column of isolation regions to define the polysilicon floating gates of the memory cells in a corresponding array column, each polysilicon floating gate having ONO formed thereon;

forming a second layer of polysilicon over the structure resulting from aforementioned steps; and

in a third mask/etch step, patterning the second layer of polysilicon utilizing a third photoresist mask to define a plurality of word lines running in the x-direction, one such word line running perpendicular to and overlying the polysilicon floating gates in each array row.

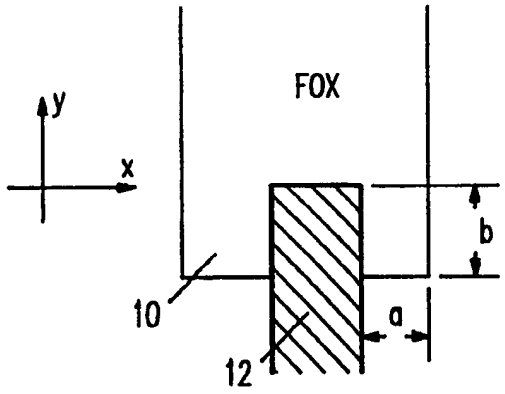

FIG. 1A
(PRIOR ART)

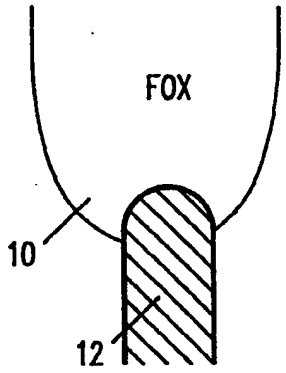

FIG. 1B
(PRIOR ART)

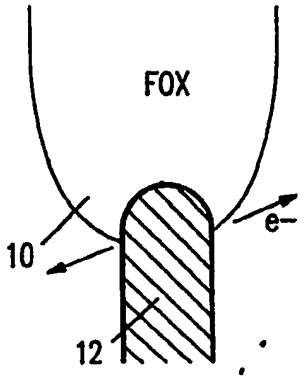

FIG. 1C
(PRIOR ART)

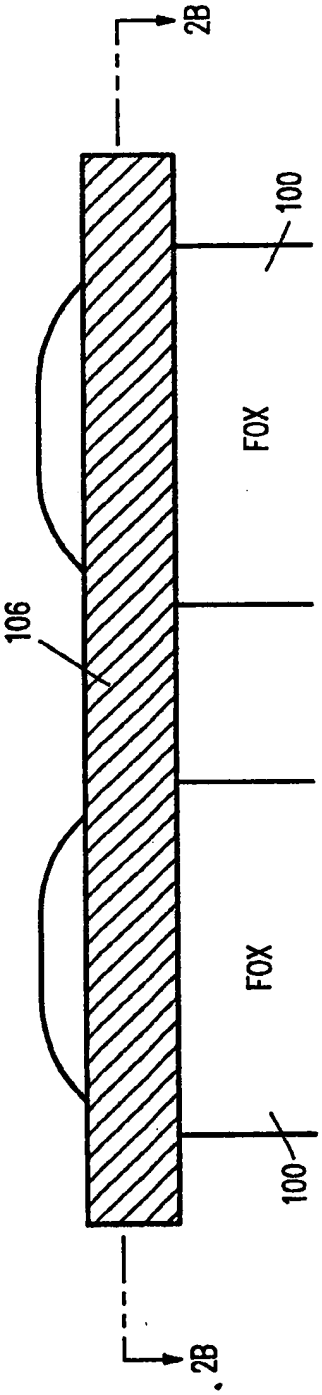
2B
100
FOX
106
FOX
100
2B

FIG. 2A

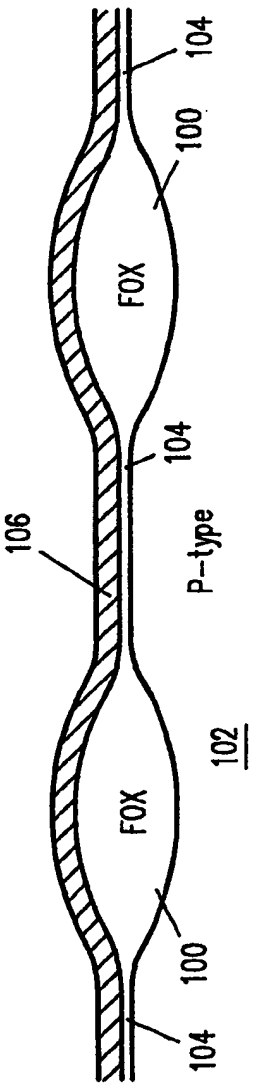
104
100
FOX
104
106
P-type
102
FOX
100
104

FIG. 2B

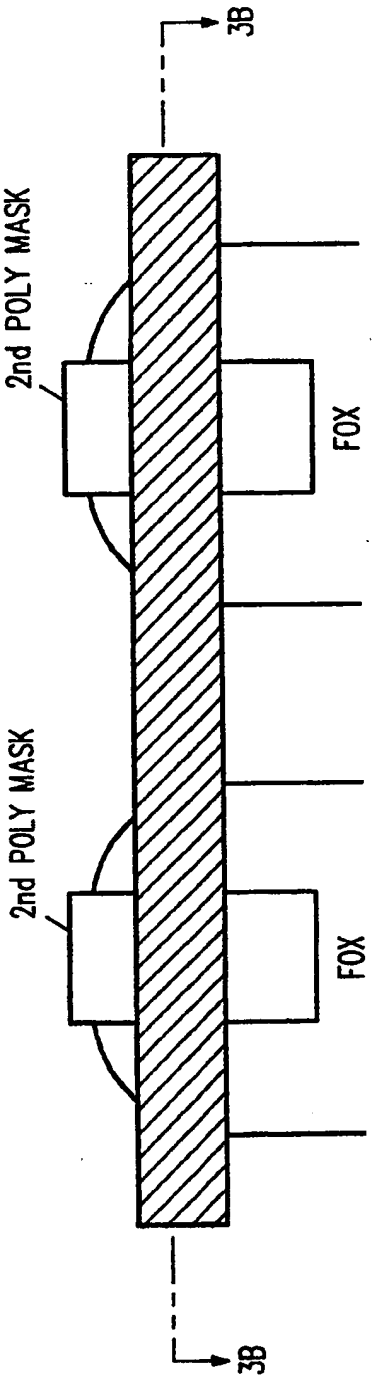
3B
2nd POLY MASK
FOX
2nd POLY MASK
FOX
3B

FIG. 3A

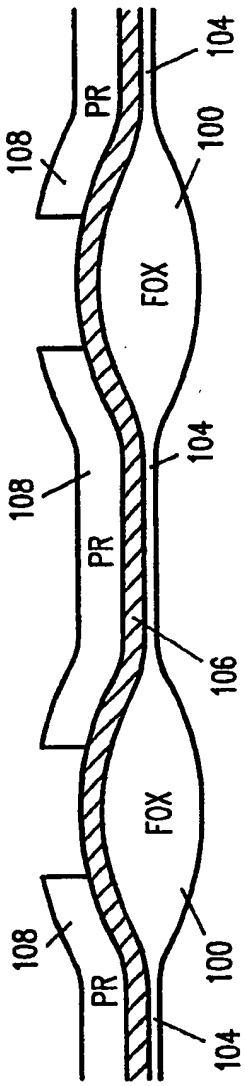
104
PR
108
100
FOX
104
108
PR
106
FOX
108
PR
100
104

FIG. 3B

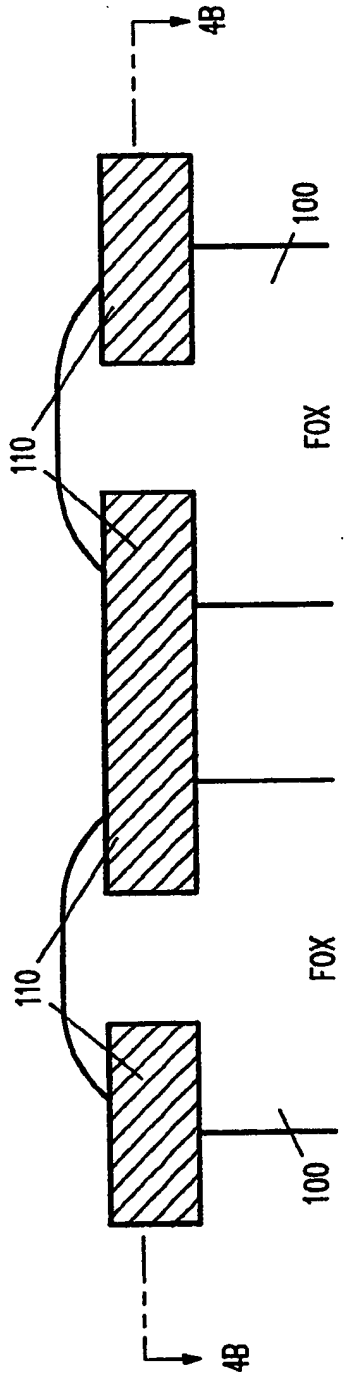

FIG. 4A

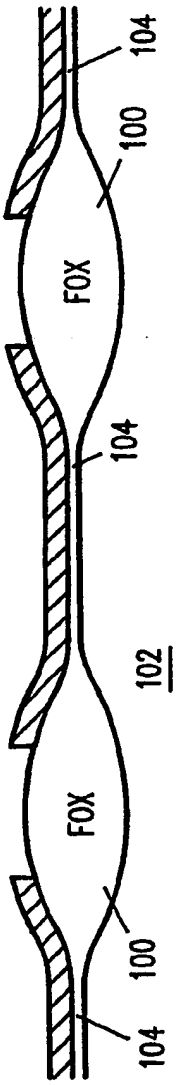

FIG. 4B

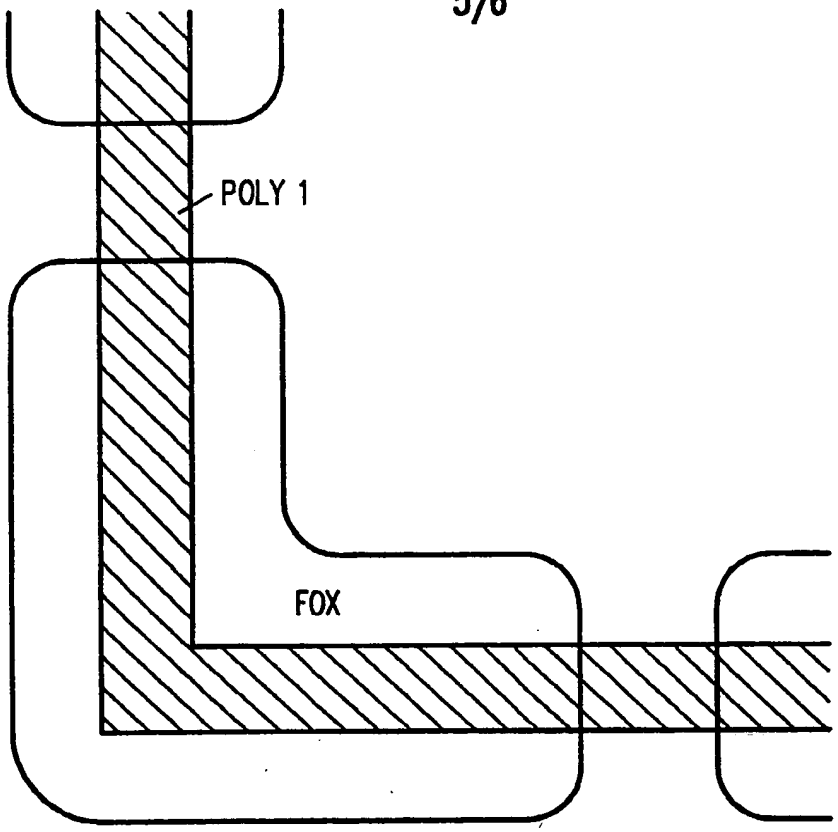

FIG. 5A

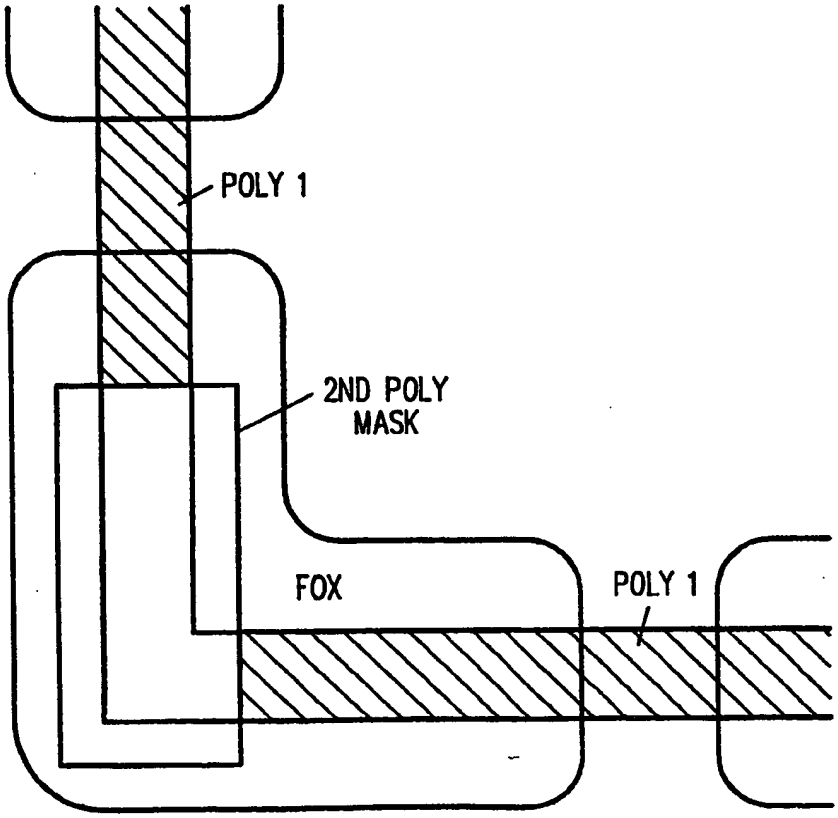

FIG. 5B

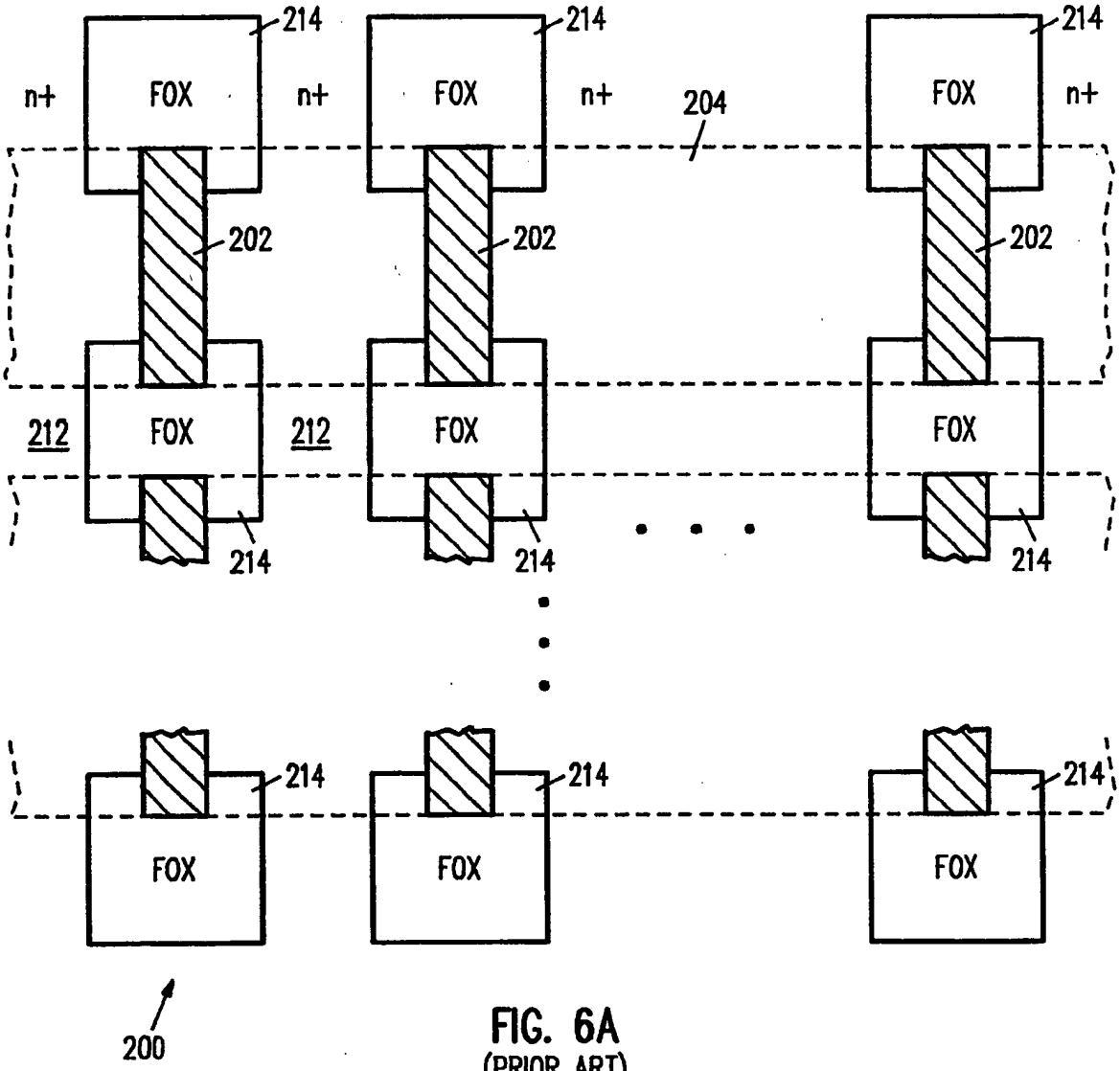

FIG. 6A
(PRIOR ART)

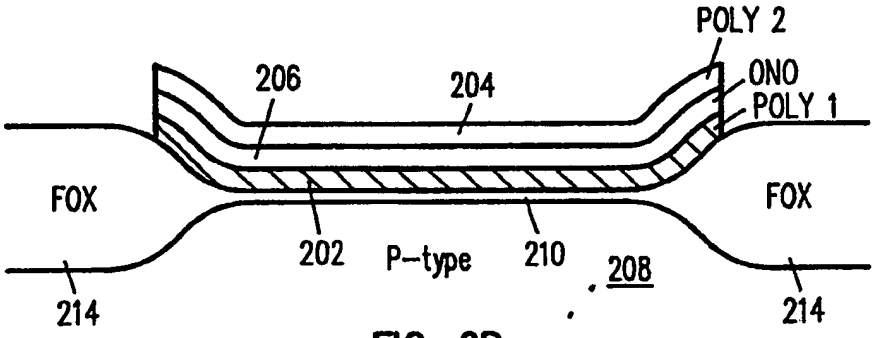

FIG. 6B
(PRIOR ART)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/.. 94/06224

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H01L21/82 H01L21/90

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,5 103 274 (D.N.TANG ET AL.) 7 April 1992 see column 1, line 59 - column 2, line 6 see column 4, line 8 - column 5, line 37	1,2
A	EP,A,0 187 278 (K.K.TOSHIBA) 16 July 1986 see page 6, line 20 - page 10, line 2	1-3

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Date of the actual completion of the international search	Date of mailing of the international search report
7 September 1994	27. 09. 94

Name and mailing address of the ISA	Authorized officer
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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/ 94/05[illegible]

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-5103274	07-04-92	US-A- 5120671	09-06-92
EP-A-0187278	16-07-86	JP-A- 61136274	24-06-86
		DE-A- 3586822	17-12-92
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		US-A- 4768080	30-08-88